High-Resolution Wideband Noise Shaping ADC with 100 MHz Bandwidth

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ABSTRACT

This paper presents a wideband noise shaping delta-sigma modulator for signal bandwidth of 100 MHz. The proposed modulator loop filter is fifth order, while the quantizer is a 4-bit. The modulator investigated for topologies of cascade of integrator and multiple feedback (CIFB) and cascade of integrator with multiple feedforward (CIFF). Both modulators utilize out-of-band gain (OBG) of 4 and oversampling ratio of 16 and can achieve signal-to-noise ratio (SNR) of 108 dB.The CIFF topology signal transfer function (STF) peaking compared to the CIFB topology of CIFB. The noise transfer function (NTF) of the modulator shows the accurate noise shaping considering ideal operational amplifier in the integrators. The modulator also implements NTF zero optimization technique to reduce further in-band quantization noise. The DC gain causes reduction of resolution of the modulator, so maximum DC gain amplifier are used in the integrator. Limited slew-rate issues for all the integrators are discussed. The circuit non-idealities like thermal noise and flicker noise also simulated at MATLAB. An extra amplifier for the CIFF topology also discussed and trade-off for the higher performance of the modulator. The CIFB topology provides higher stability for the higher order of loop filter, so CIFB topology also considered. Therefore, the modeling and MATLAB simulation shows that the modulator can achieve SNR of 108 dB at oversampling ratio (OSR) of 16 with four-bit quantizer for signal bandwidth of 100 MHz.

Keywords: CIFF, CIFB, Noise Transfer Function, Signal Transfer Function, OBG.

1. INTRODUCTION

Due to increased demands in wireless communication application for low power analog-to-digital role becomes more critical. Higher dynamic range is demanded with large signal bandwidth. Typically, Nyquist ADCs, are popular for higher signal bandwidth [1,2]. Recently the delta-sigma modulator gaining popularity for higher signal bandwidth applications. While the continuous-time delta-sigma modulator have key advantages does not require anti-aliasing filter and requires much lower gain-bandwidth. Discreate-time delta-sigma modulator have switched-capacitor implementation with components of capacitor, switches, and operational amplifier as an integrator. The continuous-time (CT) implementation uses resistor and capacitor with operational amplifier as integrator. It is well known that Nyquist pipeline ADC require accurate inter-stage gain, that determine high-gain wideband residue amplifier and calibration technology, leads to complexity and power efficiency employing noise shaping and oversampling. However, the requirement of oversampling ratios (OSRs), that is typically small [3-6]. The delta-sigma modulator more than 50 MHz getting popularity due to increased demands in portable system. The discrete-time implementation quite popular due to high accuracy but smaller bandwidth. The demand for higher bandwidth rising with

increased resolution. The challenges due to smaller OSRs due to the reason of process limited clock rate. To reach sufficient higher dynamic range, higher order noise shaping needs to be implemented by increasing the noise transfer function order, that is conventionally performed by loop filter cascade and generally equal or greater than three or more required. At the same time increased order of the loop filter causes stability issues [7]. A wideband continuous-time third order with 4-bit quantizer delta-sigma modulator designed for signal band of 100MHz can achieve dynamic range of 80-dB in 40 nm CMOS Technology at supply voltage of 1.2 V with power consumption of 69.7 mW. The modulator uses three-stage feedforward amplifier with miller compensation. The first integrator has unity gain bandwidth of 3.6 GHz and phase margin of 57 degree including all loading effect with power consumption of 10.5mW from power supply of 1.2V. The second and third integrator adopts the similar structure of the amplifier with scaled bias currents, that results in achieving unity gain bandwidth of 4.7 GHz and 3.3 GHz respectively. The phase margin for second and third integrator is 58 degree and 57 degrees and consuming power of 4.3mW and 17.3mW respectively. The power breakdown shows that loop filter consumes more than 46 % of the powers with total modulator power of 69. 7mW. While the 4-bit quantizer implemented as 4-bit flash ADC with each cell uses preamplifier due to smaller signal swing in front of quantizer. The digital-to-analog converter (DAC) is implemented using current steering unit element. Finally, the modulator can achieve signa-to-noise-plus-distortion ratio (SNDR) of 76dB and DR of 84 dB for signal bandwidth of 100 MHz for 40 nm CMOS Technology [8]. A CT modulator with third order loopfilter with preliminary sampling and quantization scheme in backend sub-ranging multi-bit quantizer can achieve SNDR of 72 dB for signal bandwidth of 100 MHz. The cascade of integrator with multiple feedforward topology used to take advantage of single DAC. While segmented non-return to zero (NRZ) DAC used for the feedback. The excess loop delay [ELD] compensation implemented around the second integrator. The modulator total power consumption is 16.3mW, while the loop filter integrators consumes 9.4mW, DAC consumes 3.5mW, quantizer 1.4mW and CLK and digital consumes 2mW respectively in 28 nm CMOS Technology sampling at 2GS/s. The modulator can achieve SNDR of 72.6dB, SNR 73.2 dB and dynamic range of 76.3 dB respectively for signal bandwidth of 100MHz in 28nm CMOS Technology [9]. Another high bandwidth CT delta-sigma modulator with signal bandwidth of 125MHz proposed based on VCO based integrators. The modulator uses VCO based quantizer and segmented phase-domain ELD compensation. The loopfilter is active RC integrator based, while modulator topology is cascaded of integrator with multiple feedforward (CIFF). The first integrator operational amplifier unity gain frequency is four times to sampling frequency. The second integrator operational amplifier unity gain frequency is three times to the modulator sampling frequency. While the third RC integrator operational amplifier unity gain frequency will be three times to sampling frequency. Finally, the third order modulator with VCO based quantizer can achieve SNDR of 71.9 dB and dynamic range of 74.8dB for signal band of 125MHz with power consumption of 54mW sampling frequency of 2.15GHz with OSR of 8.6 in 16nm CMOS Technology [10]. A CT Multi-stage Noise Shaping (MASH) modulator designed for signal band of 465MHz in 28 nm CMOS Technology. A 1-2

MASH topology is adopted to achieve aggressive noise shaping with higher stability at much lower OSR of 8.6. The first stage is a first order modulator to reduce the power amplifier for given thermal noise requirement. The first stage consists of an active RC integrator, quantizer with 17-level and current steering DAC and capacitive DAC. The second stage consists of an active-RC resonator, flash ADC of 17-levels, current steering DAC and capacitive DAC used to provide fast direct feedback. The second stage uses feedback topology to minimize STF peaking and the input full-scalr second stage is scaled down to provide an interstage gain of six to minimize the overall quantization noise floor while preventing the residue of the first stage from saturating the second stage [11].

This paper proposed a wideband noise shaping delta-sigma modulator for signal bandwidth of 100 MHz. The proposed modulator loop filter is fifth order, while the quantizer is a 4-bit. The modulator investigated for topologies of cascade of integrator and multiple feedback (CIFB) and cascade of integrator with multiple feedforward (CIFF). Both modulators utilize out-of-band gain (OBG) of 4 and oversampling ratio of 16 and can achieve signal-to-noise ratio (SNR) of 108 dB. The CIFF topology signal transfer function (STF) peaking compared to the CIFB topology of CIFB. The noise transfer function (NTF) of the modulator shows the accurate noise shaping considering ideal operational amplifier in the integrators. The modulator also implements NTF zero optimization technique to reduce further in-band quantization noise. The DC gain causes reduction of resolution of the modulator, so maximum DC gain amplifier are used in the integrator. The CIFB topology provides higher stability for the higher order of loop filter, so CIFB topology also considered. Therefore, the modeling and MATLAB simulation shows that the modulator can achieve SNR of 108 dB at oversampling ratio (OSR) of 16 with four-bit quantizer for signal bandwidth of 100 MHz.

After the introduction, the second section discuss the design of the modulator design with CIFB and CIFF structure, while the third section describes the modulator non-idealities of the modulator and explain the operational amplifier for integrator for the fifth-order 4-bit quantizer for CT design implementation. Finally, the section four concludes the paper.

2. MODULATOR DESIGN

A fifth-order multi-bit modulator modeled using Delta-Sigma Toolbox [12]. The cascade of integrator with multiple feedback (CIFB) as well as cascade of integrators with multiple feedforward (CIFF) evaluated with out-of-band-gain (OBG) of 4 with an oversampling ratio of 16 without NTF zero optimization technique. The CIFB topology can achieve SNR of 94 dB while the CIFF topology can achieve SNR of 92 dB. The NTF zero optimization causes more in-band quantization noise shaped to out-of-band and results in improved performance. With NTF zero optimization technique both modulator topologies can achieve SNR of 108 dB with similar OSR of 16 and OBG of 4. The CIFB modulator coefficient obtained from the toolbox shown in Table-I. This coefficient represents the ratio of capacitors at the switched-capacitor implementation, for the discrete-time implementation of the modulator. While for the CT implementation these coefficient needs to be converted into the CT equivalent coefficient [13]. Then these converted coefficients will be used to choose the resistor and capacitor ratio considering the sampling frequency.

Those coefficients which are not mentioned, have value zero. The Table II shows the coefficients of the case of CIFF topology. The signal-transfer function (STF) and noise transfer function (NTF) of the modulator is shown in Figure 1. While the Figure 2 shows the output power spectral density (PSD) plot. The fifith-order noise shaping is shown in the Figure 2, while the NTF zero optimization is shown very close to signal bandwidth. The PSD plot shows that CIFB topology of the modulator can achieve SNR of 108 dB with an OSR of 16. The output states of the integrator are shown in the Figure 3. Due to the CIFB topology the swing inside the loop filter is large and requires large DC gain amplifier for the integrators. All operational amplifier inside the loop filter is ideal have infinite gain to suppress the quantization noise in the signal band of the modulator. The Figure 4 shows the OBG value set to 4 for the case of NTF,

Table I : CIFB Topology Cofficients

Parameters	Values
a1	0.11
a2	0.70
a3	2
a4	3.1
a5	2.6
g1	0.01
g2	0.03
b1	0.11

Table II: CIFF Topology Coefficients

Parameters	Values
a1	2.66
a2	3.14
a3	1.98
a4	0.64
a5	0.04
b1	1
g1	0.01
g2	0.03
c1	1
c2	1
c3	1
c4	1
c5	1

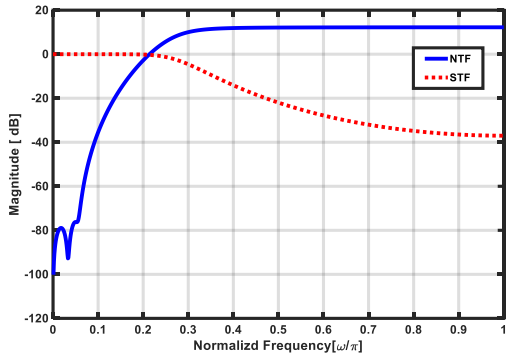

Figure 1: STF and NTF plot (CIFB)

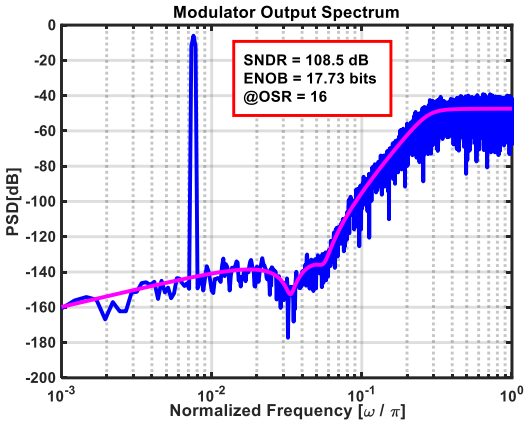

Figure 2: Output PSD plot (CIFB)

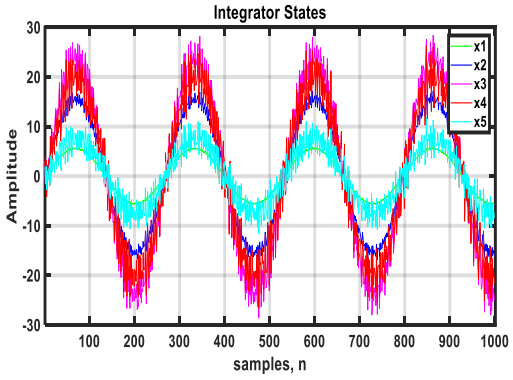

Figure 3: Output states of the integrators

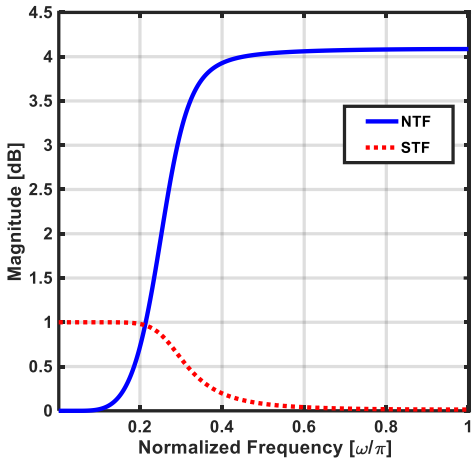

Figure 4: STF and NTF plot (CIFB)

while the STF have unity gain values according to the simulation environment.

3. NON-IDEALITIES SIMULATION

To realize the practical implementation of the modulator, non-idealities need to be simulated so that circuit designed can get an estimate of the performance. The simulation environment SDToolbox [14] which simulates the circuit non-idealities are used. This section will discuss about the circuit non-idealities like thermal noise or kT/C, flicker noise, finite operational amplifier gain, finite slew-rate, finite gain-bandwidth (GBW).

NOT DONE

4. CONCLUSION

A fifth-order multi-bit modulator investigated for topologies of cascade of integrator and multiple feedback (CIFB) and cascade of integrator with multiple feedforward (CIFF). Both modulators utilize out-of-band gain (OBG) of 4 and oversampling ratio of 16 and can achieve signal-to-noise ratio (SNR) of 108 dB. The CIFF topology signal transfer function (STF) peaking compared to the CIFB topology of CIFB. The noise transfer function (NTF) of the modulator shows the accurate noise shaping considering ideal operational amplifier in the integrators. The modulator also implements NTF zero optimization technique to reduce further in-band quantization noise. The DC gain causes reduction of resolution of the modulator, so maximum DC gain amplifier are used in the integrator. Limited slew-rate issues for all the integrators are discussed. The circuit non-idealities like thermal noise and flicker noise also simulated at MATLAB. An extra amplifier for the CIFF topology also discussed and trade-off for the higher performance of the modulator. The CIFB topology provides higher stability for the higher order of loop filter, so CIFB topology also considered. Therefore, the modeling and MATLAB simulation shows that the modulator can achieve SNR of 108 dB at oversampling ratio (OSR) of 16 with four-bit quantizer for signal bandwidth of 100 MHz

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